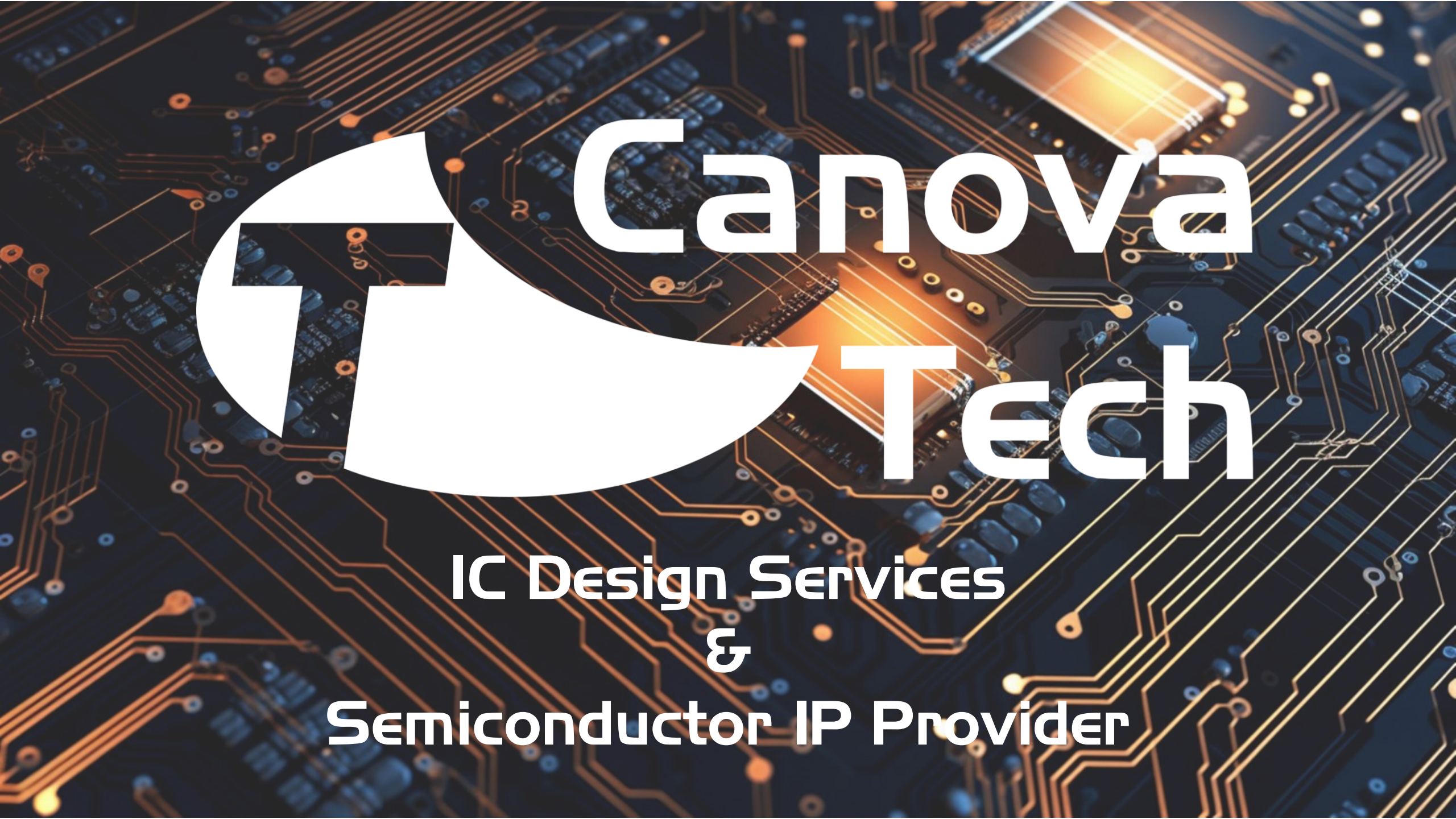

Canova
Tech
IC Design Services
&
Semiconductor IP Provider

Snapshots & Memberships

Established in 2005

Based in Italy
- HQ in Padua
- 2nd Design office in Genoa

30 employees

Infrastructures
- Industry-Std EDA tools
- IC qualification Lab

Privately held

Active member and contributor of industry and telecommunication standards

IEEE Advancing Technology for Humanity

OPEN ALLIANCE

USB Enabling Connections™

GSA Where Leaders Meet

IC Design Service & IP Licensing

Mixed-signal design support

- On-site & off-shore
- Under the direction of the customer's Project Leader
- Mixed-signal design layout and verification
- VPN to customer's servers

Custom block design

- Block spec co-development and review
- Complete block design, layout and verification according to the specs
- Delivery of design views, test specifications, integration guidelines, complete database
- Weekly calls and dedicated meetings

End-to-end ASIC Design

- Architectural study and feasibility assessment
- IC spec co-development and review
- Complete IC design
- Complete IC testing and characterization
- Engineering support during transfer to production
- Complete IC dababase delivery
- Weekly calls and dedicated meetings

Standard IP customization

- Block spec from Canova's IPs
- Complete IP design, layout and verification according to the specs
- Delivery of design views, test specifications, integration guidelines
- IP test chip design and characterization
- Weekly calls and dedicated meetings

Wireline Standard IP

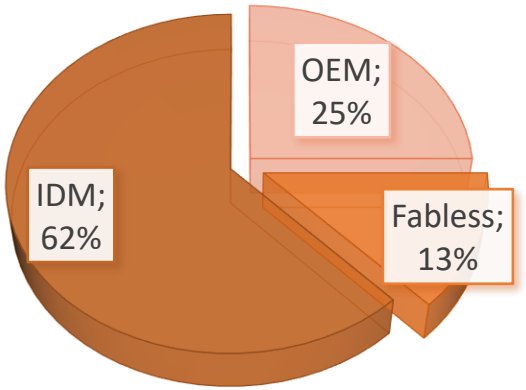
- 802.3cg 10BASE-T1S Single-Pair MultiDrop Automotive and Industrial Ethernet PHY IP
- USB2 FS PHY and dedicated RTL stacks
- USB2 clock-less oscillator (for device side)
- USB Power Delivery PHY and Stack for USB Type-C
- Embedded USB2 (eUSB2) Repeater IP
- 802.3bw 100BASE-T1 Single-Pair Automotive Ethernet PHY IP

Design Service | IP Licensing

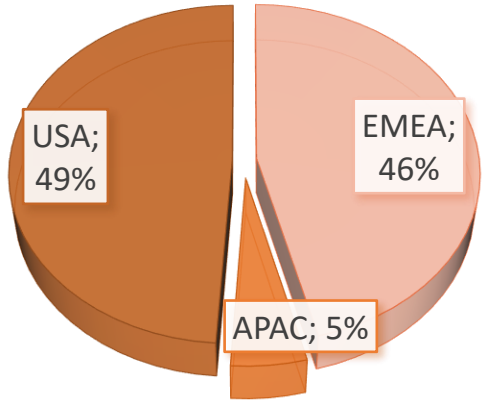
Canova Tech

Clients & Quality

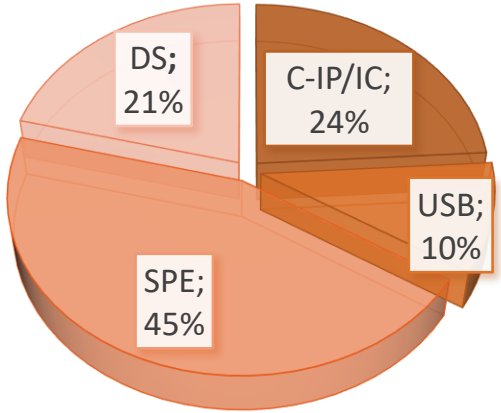
Working with market-leaders and innovators worldwide



Client type split



Client geographical split



Project type split

- Management system as per **ISO 9001:2015**
- **IATF 16949** compliance

Canova Tech is ISO 9001 Certified by TÜV NORD since 2014

Silicon processes experience

BCD

- 350 nm
- 180 nm
- 130 nm

High voltage options

CMOS

- 65 nm
- 40 nm
- 32 nm
- 28 nm
- 22 nm

FinFET

- 7 nm
- 5 nm
- 3 nm
- Below

Silicon-proven custom design

Power management

Linear and switching

- Low-drop regulators (incl. cap-less)
- Buck converters
- Boost converters
- AC/DC active bridge
- Battery operated
- Energy harvesting

Auxiliary & Monitors

Auxiliary and monitors

- Oscillators and timing
- Bandgap voltage references
- Temperature sensors and monitors
- Process monitor
- Leakage monitor
- Current and voltage monitors

AFE+AD & DA+Drivers

AD/DA converters

- Industrial IO-Expander AD
- Imagers AD and serializers
- UWB baseband AD
- IVT monitor AD
- Motor/MEMS drivers

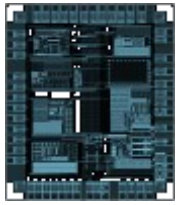
FinFET

A/MS & Mask design

- Skilled team of A/MS and Mask designers with 20.000 hours of cumulative experience in N7, N5, N3 and N2

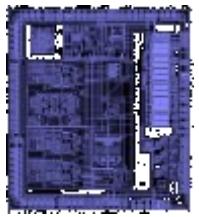
Custom IC Examples

Harvesting Boost DCDC



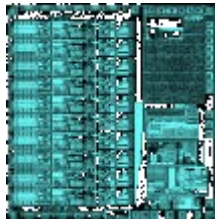
Ultra Low Power Digital Pen IC

Implantable Pacemaker

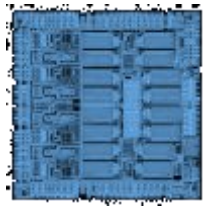


Implantable Pressure Monitor

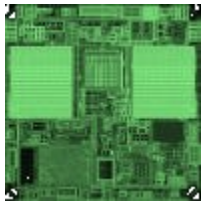
10ch Industrial Sensor I/F



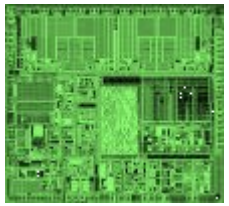
Pulse Oximeter



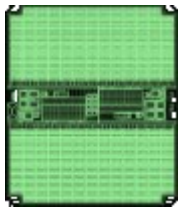
Street Lighting LED Driver



Solar Panel Junction Box

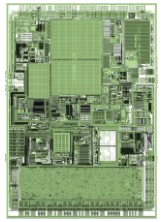


High Speed Laser Drv

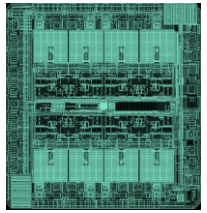


Touch Panel Controller

PoE PD Side



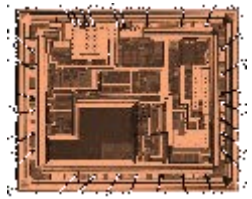
PoE 8ch PSE Side



USB-PD 1 PHY

USB-PD 3 TCPC PHY

USB-PD 3 TCPC PHY



10BASE-T1S Ethernet PHY

100BASE-T1 Ethernet PHY

InkJet PrintHead

Silicon-proven wireline technologies

SPE

Automotive & Industrial single-pair Ethernet

- IEEE 802.3cg, 10BASE-T1S dPHY + OA-TXC
- IEEE 802.3cg, 10BASE-T1S PHY & OA-MACPHY
- IEEE 802.3da, 10BASE-T1M (under standardization)
- OPEN Alliance TC14, OA-TXC Interface
- OPEN Alliance TC14, OA-MACPHY Interface
- OPEN Alliance TC14-TC16, Sleep/Wake
- IEEE 802.3bw, 100BASE-T1 PHY

USB

Consumer & Automotive universal serial bus

- USB2, USB2 PHY and XTAL-less oscillator
- eUSB2, eUSB2 Repeater
- USB-PD, USB-PD3 PHY
- USB-PD, USB-PD3 Protocol Stack
- USB Type-C, USB-C Interface
- USB TCPC, Type-C Port Controller

Custom

Custom interfaces

- NFC-like (implantable medical)
- Custom powerline (junction box)

SerDes

Consumer SerDes (Transmitter & Receiver)

- 3.5 Gbit/sec HDMI/DP/MHL
- 6 Gbit/sec HDMI/DP/eDP
- 0.5 Gbit/sec LVDS (image sensor)

Canova Tech 10BASE-T1S Achievements

- Inventor of the **PLCA** (Physical Layer Collision Avoidance)
  - United States Patent 20190230705; “METHOD FOR PREVENTING PHYSICAL COLLISION ON ETHERNET MULTIDROP NETWORKS”
    - Essential patent IP of the IEEE 802.3cg-2019 standard (for multi-drop operations)
- Inventor of the **Dynamic-PLCA**
  - United States Patent 12,088,058; “METHOD FOR DATA TRANSMISSION ON ETHERNET MULTIDROP NETWORKS IMPLEMENTING DYNAMIC PHYSICAL LAYER COLLISION AVOIDANCE”
    - Approved by the IEEE 802.3da working group as baseline for the standard
- IEEE 802.3cg-2019 standard editor and contributor
  - Clause 147 (PCS, PMA and Management)
  - Clause 148 (PLCA Reconciliation Sublayer)
- OPEN Alliance active contributor in all open discussions (Interoperability, compliance test, Wake/Sleep, SQI, Cable Diagnostic, PLCA diagnostic)
  - Proponent and editor of the Transceiver Interface
  - Proponent of the MACPHY SPI Interface
  - Proponent of the Topology Discovery feature

Open Positions

IC Layout Design Engineer

Responsibilities

- Collaborate with circuit design teams to plan and schedule work.
- Negotiate layout trade-offs to build complex analog layouts.
- Recognize and correct failure-prone circuit and layout structures.
- Run design verification tools to ensure quality at all levels of chip design.
- Interpret LVS, DRC, and ERC reports to expedite layout completion.
- Meet engineering specifications by working closely with circuit design teams.
- Utilize advanced CAD tools and mask design knowledge to deliver robust layouts.

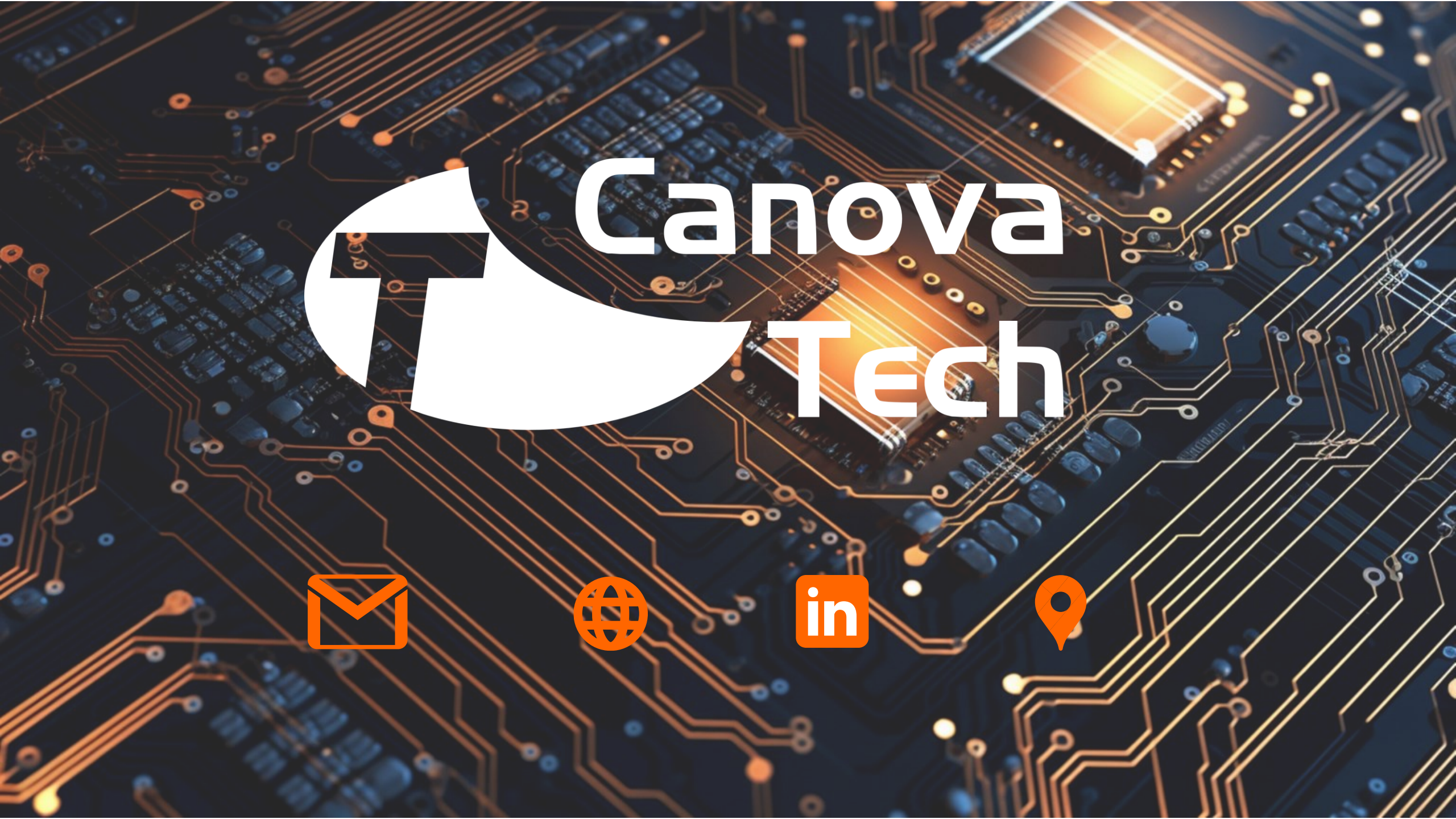
Requirements

- Bachelor's Degree. Electronic Engineering, Physics or similar.
- Good proficiency in Italian & English.
- Comfortable with commuting to the job's location: Genova (GE), Italy.

Proposal

- Permanent employment.

We look forward to meeting you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